In the Claims

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1-10. (Canceled)

11. (Previously Presented) A method comprising:
forming a window in a layer on a substrate to expose a region of the substrate;
forming defects in the region by implanting electrically neutral species; and
depositing a silicon layer on the region at a temperature of less than 750 °C prior to annealing the substrate.

12. (Canceled)

13. (Original) The method of claim 11, comprising depositing the silicon layer in a reducing environment.

14. (Original) The method of claim 13, wherein the reducing atmosphere comprises a mixture of hydrogen and silane.

15. (Original) The method of claim 11, comprising depositing the silicon layer at a pressure of less than about 0.1×10^5 Pa.

16-19. (Canceled).

20. (Previously presented) The method of claim 11, comprising forming defects by implanting fluorine atoms.

21. (Previously presented) The method of claim 11, further comprising depositing an oxide layer having a thickness of less than 10 nm on the surface of the region prior to the implantation step and removing the oxide layer after the implantation step.

22. (Original) The method of claim 11, comprising forming defects by an etching process that directs ions toward the region.

23. (Original) The method of claim 11, comprising forming interstitial defects in the region with an atomic proportion of one defect per one hundred silicon atoms.

24. (Original) The method of claim 11, wherein the region has a depth of less than 5 nm.

25. (Canceled)

26. (Currently Amended) The method of claim 11 ~~25~~, wherein the window has a width of less than 5 microns.

27. (Original) The method of claim 11, wherein the silicon layer has a different crystalline orientation than the substrate.

28. (Original) The method of claim 11, wherein the substrate is a silicon substrate.

29. (Original) The method of claim 11, wherein the substrate is a single crystal.

30. (Original) The method of claim 11, wherein the silicon layer is a single crystal.

31. (Original) The method of claim 11, wherein the region comprises an emitter of a bipolar transistor.

32. (Currently Amended) A method comprising:

forming a window in a layer on a single-crystal silicon substrate to expose a region of the substrate;

forming defects in the region of by implanting electrically neutral species; and

depositing a single-crystal silicon layer at a temperature of less than 750 °C on the region prior to annealing the substrate, the silicon layer having a different crystalline orientation than the substrate.

33-35. (Cancelled)

36. (Original) The method of claim 32, comprising depositing the silicon layer in a reducing environment including a mixture of hydrogen and silane.

37. (Original) The method of claim 32, comprising depositing the silicon layer at a pressure of less than about 0.1×10^5 Pa.

38. (Canceled)

39. (Previously presented) The method of claim 32, further comprising depositing an oxide layer having a thickness of less than 10 nm on the region prior to the implantation process.

40. (Original) The method of claim 32, comprising forming interstitial defects in the region with an atomic proportion of one defect per one hundred silicon atoms.

41. (Original) The method of claim 32, wherein the region has a depth of less than 5 nm.

42-44. (Canceled)

45. (Previously presented) The method of claim 11, comprising depositing the silicon layer at a pressure of about 0.1×10^5 Pa.

46. (Previously presented) The method of claim 32, comprising depositing the silicon layer at a pressure of about 0.1×10^5 Pa.

47. (Previously presented) The method of claim 11, comprising depositing the silicon layer at conditions corresponding to epitaxial deposition conditions but at a temperature of less than 750 °C.

48. (Previously presented) The method of claim 32, comprising depositing the silicon layer at conditions corresponding to epitaxial deposition conditions but at a temperature of less than 750 °C.

49. (Previously presented) The method of claim 11, wherein the electrically neutral species comprise atoms.

50. (Previously presented) The method of claim 32, wherein the electrically neutral species comprise atoms.

51. (Previously presented) The method of claim 11, comprising depositing the silicon layer on the region at a temperature between 600 °C and 700 °C.

52. (Previously presented) The method of claim 32, comprising depositing the silicon layer on the region at a temperature between 600 °C and 700 °C.